Shortie VHDL for Synthesis

Emerging applications ranging from AI for IoT, embedded vision, hardware security, 5G communications, and industrial/automotive automation are redefining hardware requirements for developers designing products that operate at the network Edge.

To support these applications, Edge devices need hardware options that offer:

• Low power consumption

• High performance

• High reliability

• Small form factor

• Small form factor

The design of digital circuits in this scale needs a powerful hardware description language which offers different levels of abstraction, so an engineer can create a digital hardware design in a quick and effective way. VHDL fulfils these requirements.

VHDL is a strongly typed hardware description language which prohibits typical programming mistakes in the coding phase. Usually, VHDL is used on the register transfer level (RTL) to design digital circuits of any complexity. Apart from the language constructs for synthesis, VHDL offers a wide range of functionality to describe complex verification models. Thus, it is possible verify digital designs from simple gate up to complex System-on-Chip (SoC) before going to lab tests.

This event is the online variant of the face-to-face VHDL training and teach the synthesis relevant aspects of the VHDL hardware description language based on the IEEE Std. 1076-2008 language revision including basic introduction to Test Benches. The theoretical knowledge will be deepened with demonstrations and examples presented by the trainer and labs which will be carried out by the attendees.

Course Objectives:

- Vision: Learn an all parallel computer language to describe digital circuits
- Learn VHDL-2008 language constructs mainly for synthesis
- Understand parallel execution model
- Understand how VHDL translates to gates and circuits
- Create digital circuit descriptions for FPGAs
- Run the synthesis and implementation tool flow in Lattice Radiant / Diamond Software
- Divide a design into hierarchical units
- Demonstrations, Labs and Exercises

Agenda

VHDL Concept and Design Units

- Design Paradigm
- Libraries and compiled units
- Packages
- Entity
- Architecture
- Configuration

Data Types

- Scalar
- Complex Types
- Attributes

Naming Conventions and Declarations

Statements and Assignments

Sequential Statements

- Statements
- Sub Programs

Signals

- Declaration
- Signal Assignments inside Processes

Concurrent Statements

Structural Descriptions

- Hierarchy
- Use of Packages
- Generics

Libraries and Packages

- Packages
- Libraries

Labs

- The theoretical content is supplemented by exercises presented by the trainer and carried out by the participant.

Lab1: Simple Counter

Lab2: Finite State Machines

Applicable Technologies

- all Lattice Semiconductor FPGAs and CPLDs

Software / Hardware used

- Lattice Semiconductor Radiant Design Software,
- Lattice Semiconductor CrossLink-NX Evaluation Board

Prerequisites

- Basic Knowledge in digital circuit design is welcome.

Workshop Format and Duration

- Shortie, 4 hours

Participant Documents provided

- Presentation Work-Book
- Exercise Lab-Book
