On-Line Intensive Workshop

Crosslink NX

Emerging applications ranging from AI for IoT, embedded vision, hardware security, 5G communications, and industrial/automotive automation are redefining hardware requirements for developers designing products that operate at the network Edge.

To support these applications, Edge devices need hardware options that offer:

• Low power consumption

• High performance

• High reliability

• Small form factor

CrossLink™-NX family of low-power FPGAs can be used in a wide range of applications, and are optimized for bridging and processing needs in Embedded Vision applications – supporting a variety of high bandwidth sensor and display interfaces, video processing and machine learning inferencing. It is built on Lattice Nexus FPGA platform, using low-power 28 nm FD-SOI technology. It combines the flexibility of an FPGA with the low power and high reliability (due to extremely low SER) of FD-SOI technology.This event is the online variant of the face-to-face workshop “CrossLink NX” teaches the user in the way, the FPGA how building blocks of the CrossLink NX Series work and how they can be used most effectively.

The emphasis of this workshop is put on the thorough discussion of the common architectural building blocks. After an overview, detailed explanations are given to the functional blocks such as e.g. PFU Blocks I/O Buffer for system- or source synchronous data transmission in single or double data rate mode, DSP etc. Due to its crucial role in an FPGA design, special attention is given to the clocking resources and clock structure. To top the content off, dedicated hardware resources such as Memory Interfaces, MIPI IPs and PCIe will be introduced.
Moreover, suitable coding techniques get explained throughout the class to allow synthesis to produce the best possible implementation results based on the target device’s resources

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Course Objectives:

- Describe all the functionality of the PFU construction of the CrossLink NX series FPGAs
- Specify the PFU resources and the available configurations for the CrossLink NX series FPGAs
- Define the RAM, FIFO, and DSP resources available for the CrossLink NX series FPGAs
- Properly design for the I/O block and SERDES resources in the CrossLink NX series FPGAs
- Identify the PLL, and clock routing resources included with these families
- Identify the hard resources available for implementing high-performance DDR3 physical layer interfaces
- Properly code your HDL to get the most out of the CrossLink NX series FPGAs
- Describe the additional dedicated hardware for all the CrossLink NX series members

- Demonstrations, Labs and Exercises

Agenda

PFU Blocks

- Slice
- Modes of Operation
  - Logic Mode
  - Ripple Mode
  - RAM Mode
  - ROM Mode

Routing

- Clocking Structure
- Global PLL
- Clock Distribution Network
- Primary Clocks & Edge Clock
- Clock Divider
- Clock Center Multiplexor Blocks
- Dynamic Clock Select & Dynamic Clock Control
- DDRDLL

SGMII Clock Data Recovery (CDR)
sysMEM Memory

- sysMEM Memory Block
- Bus Size Matching
- RAM Initialization and ROM Operation
- Memory Cascading
- Single, Dual and Pseudo-Dual Port Modes
- Memory Output Reset

Large RAM
sysDSP

- sysDSP Approach Compared to General DSP
- sysDSP Architecture Features

ALUREG
Programmable I/O (PIO)
Programmable I/O Cell (PIC)

- Input Register Block
  - Input FIFO
- Output Register Block

Tristate Register Block
DDR Memory Support

- DQS Grouping for DDR Memory

- DLL Calibrated DQS Delay and Control Block (DQSBUF)

sysI/O Buffer

- Supported sysI/O Standards
- sysI/O Banking Scheme

Analog Interface

- Analog to Digital Converters
- Continuous Time Comparators

Device Configuration

- Enhanced Configuration Options
  - TransFR (Transparent Field Reconfiguration)
  - Dual-Boot and Multi-Boot Image Support

Single Event Upset (SEU) Support
On-Chip Oscillator
User I²C IP
MIPI D-PHY Blocks
Peripheral Component Interconnect Express (PCIe)

Labs

- The theoretical content is supplemented by exercises presented by the trainer and carried out by the participant.

Applicable Technologies

- Lattice Semiconductor CrossLink NX Series FPGAs

Software / Hardware used

- Lattice Semiconductor Radiant Design Software,
- Lattice Semiconductor CrossLink-NX Evaluation Board

Prerequisites

- Basic Knowledge in digital circuit design is welcome.

Workshop Format and Duration

- Online, 3 days with 4 hours per day

Participant Documents provided

- Presentation Work-Book
- Exercise Lab-Book
