On-Line Intensive Workshop Timing Constraints

FPGA Designs usually require the proper and complete specification of timing requirements.
Timing constraints may be used to influence and guide the placement of design elements and signal routes between placed elements in order to meet design performance requirements. The two general types of timing constraints are global and path-specific. Global timing constraints cover all paths within the logic design. Path-specific constraints cover specific paths.

This On-Line LEC2 workshop "Timing Constraints" teaches the attendee how to use Timing Constraints most effectively. After an overview, detailed guidelines on definition of timing constraint are given.

Moreover, suitable use Cases and examples get explained throughout the class to allow to produce the best possible implementation results based on the target device's timing requirements.

Course Objectives:

- Identify and constrain system clocks.
  - The timing constraint process should start with the specification of the global timing constraints for all identified system clocks.
- Identify and create signal path groups.
  - The two primary types of path groups are global and specific. A global group typically includes a group of paths between registers, input paths, and output paths. Specific paths are mostly static or combinatorial paths, paths between clock domains, or multicycle paths.
- Assign global constraints.
  - The general rule of thumb when assigning constraints is to use global constraints for primary coverage of a majority of the design paths. With access to timing constraints, synthesis tools may attempt to optimize the synthesized design to meet the specified timing requirements.
- Assign Timing Exceptions
- Demonstrations

Agenda

Introduction to the Radiant FPGA Design Flow

- Introduction to Radiant Timing Constraints Editor

Introduction to FPGA Timing Requirements

- The basic Idea

Introduction to Clock Constraints

- Generated Clocks
- Clock Group Constraints

I/O Constraints and Virtual Clocks

- I/O Timing Scenarios
- Source-Synchronous I/O Timing
- System-Synchronous I/O Timing

Setup and Hold Timing Analysis

Introduction to Timing Exceptions

- FALSE PATH
- MIN / MAX DELAY
- MULTICYCLE

Reading Timing Report

Timing Constraints Priority

Labs

The theoretical content is supplemented by exercises presented by the trainer and carried out by the participant.

- Introduction to Clock Constraints
- IO Constraints and Virtual Clocks
- Generated Clocks
- Introduction to Timing Exceptions

Applicable Technologies

- all Lattice Semiconductor FPGAs and CPLDs

Software / Hardware used

- Lattice Semiconductor Radiant Design Software,
- Lattice Semiconductor CrossLink-NX Evaluation Board

Prerequisites

- Basic Knowledge in digital circuit design is welcome.

Workshop Format and Duration

- On-Line, 3 days with 4 hours per day

Participant Documents provided

- Presentation Work-Book
- Exercise Lab-Book
