Webinar FPGA Design Technique

For the successful implementation of digital circuits in the FPGA, the strong knowledge of the digital circuit's basics is mandatory. The HDL based developing method simplifies the developing cycle, but for that, the developer must have the good knowledge of digital circuit design. Although most of the developers basically know the digital components like combinational and sequential and their usage, it is very important to know the FPGA architecture for which a digital design should be implemented.

After the review of combinational and sequential circuits, the design of combinatorial circuits, sequential circuits and sequential systems will be discussed.

In almost every digital design there is Clock Domain Crossing where CDC Analysis and synchronization circuits are needed, which is described.

The theoretical content is supplemented by exercises carried out by the participant.

Course Objectives:

- Describe the general structures of FPGAs
- Describe the clocking structures of FPGAs
- Understand synchronous design techniques

Agenda

Introduction to the general FPGA Architecture

- Combinatorial Resources
- Sequential Resources
- RAMs and FIFOs
- Input / Output Resources

Design for Speed

- Throughput and Latency
- Register balancing

Design for Area

- Rolling up the pipe line
- Resource sharing
- Impact of Reset

Design for Power

- Clock Control

Design for Reliability

- Synchronous vs. Asynchronous
- Synchronous Design Technique

Rules and best practices

Demos

- The theoretical content is supplemented by exercises presented by the trainer and carried out by the participant.

Applicable Technologies

- Lattice Semiconductor FPGAs

Software / Hardware used

- Lattice Semiconductor Radiant Design Software,
- Lattice Semiconductor CrossLink-NX Evaluation Board

Prerequisites

- Basic Knowledge in digital circuit design is welcome.

Format and Duration

- Webinar, 45 min. presentation and 15 min. Q&A

Participant Documents provided

- Presentation
